High-Resolution Inkjet Printing of All-Polymer Transistor Circuits

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Science **290**, 2123 (2000);
DOI: 10.1126/science.290.5499.2123

Science (print ISSN 0036-8075; online ISSN 1095-9203) is published weekly, except the last week in December, by the American Association for the Advancement of Science, 1200 New York Avenue NW, Washington, DC 20005.

it provides further evidence of the conversion of these nanostructures to Mo°. In contrast, as-deposited MoO_x composite nanowires were brittle and were subject to breaking when flexed by as little as 5°.

We conducted a survey of other metals and discovered that noble metals, including silver, platinum, and copper, do not nucleate with a sufficiently high linear density along step edges on graphite to form continuous nanowires, but instead form disconnected linear arrays of micrometer-scale metal particles. These three metals all exhibited facile electrodeposition kinetics at graphite surfaces. In contrast, several base metals, all of which exhibit slow heterogeneous electron transfer kinetics for deposition, behaved similarly to molybdenum. For example, we obtained nanowires of cadmium and nickel-molybdenum alloy by using deposition conditions analogous to those used in this study.

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10. Eq. 1 is readily derived from the expression for the deposition charge associated with the formation of a hemicylindrical solid, $Q_{dep} = (\pi r^2 nF\rho l/2M)$. For deposition with a constant current i_{dep}, $Q_{dep} = i_{dep}t_{dep}$. Eq. 1 is then obtained by solving for $r(t)$ in this equation.
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12. A more extensive version of Fig. 3 is available at www.sciencemag.org/cgi/content/full/290/5499/2120/DC1.
13. The lattice parameter for body-centered cubic molybdenum metal is 3.1472 Å. Lattice parameters for monoclinic MoO_2 are $a = 5.6096$ Å, $b = 4.857$ Å, and $c = 5.6259$ Å, and $\beta = 120.912$.

14. This work was funded by the NSF (grant DMR-9876479) and the Petroleum Research Fund of the American Chemical Society (grant 33751-AC5). We also gratefully acknowledge the financial support of the Camille and Henry Dreyfus Foundation. Finally, donations of graphite by A. Moore of Advanced Ceramics are gratefully acknowledged.

11 August 2000; accepted 13 October 2000

High-Resolution Inkjet Printing of All-Polymer Transistor Circuits

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Direct printing of functional electronic materials may provide a new route to low-cost fabrication of integrated circuits. However, to be useful it must allow continuous manufacturing of all circuit components by successive solution deposition and printing steps in the same environment. We demonstrate direct inkjet printing of complete transistor circuits, including via-hole interconnections based on solution-processed polymer conductors, insulators, and self-organizing semiconductors. We show that the use of substrate surface energy patterning to direct the flow of water-based conducting polymer inkjet droplets enables high-resolution definition of practical channel lengths of 5 micrometers. High mobilities of 0.02 square centimeters per volt second and on-off current switching ratios of 10^5 were achieved.

Semiconducting organic molecules (*1*) and polymers (*2*) can be self-assembled from solution into ordered structures with charge carrier mobilities close to that of inorganic thin-film silicon. They may form the basis of a new thin-film electronic technology, in which integrated transistor circuits are manufactured by cheap solution processing and direct printing rather than vacuum deposition and photolithographic patterning (*3*–*6*). However, this requires the development of printing techniques that provide accurate definition of all components of an integrated circuit but do not compromise the ability of the organic molecules to self-assemble. Inkjet printing (IJP) has emerged as an attractive patterning technique for conjugated polymers in light-emitting diodes (*7, 8*) and full-color high-resolution displays (*9*). The technique has not been applied to organic transistors yet, because its resolution is limited to 20 to 50 μm by statistical variations of the flight direction of droplets and their spreading on the substrate. This is not sufficient for defining source-drain electrodes of practical thin-film transistors (TFTs) without accidental electrical shorts. Channel lengths of $L = 5$ to 10 μm are required to achieve adequate drive current and switching speed.

Our approach for overcoming this problem is to confine the spreading of water-based conducting polymer ink droplets on a hydrophilic substrate with a pattern of narrow, repelling, hydrophobic surface regions that define the critical device dimensions (Fig. 1A). This surface free energy pattern on the Corning 7059 glass substrate is fabricated before TFT deposition by photolithography and O_2 plasma etching of a 500 Å polyimide film (*9*). After etching through the polyimide, the O_2 plasma renders the source-drain regions on the bare glass hydrophilic, whereas the polyimide line defining the TFT channel is protected by photoresist and remains hydrophobic. The contact angle of water on hydrophilic glass and hydrophobic polyimide is 20° to 25° and 70° to 80°, respectively. For the source-drain and gate electrodes we use a water-based ink of the conducting polymer poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid (PEDOT/PSS, Baytron P from Bayer, Krefeld, Germany). Our home-built, piezoelectric inkjet printer is equipped with an optical imaging system that allows coarse alignment (± 5 μm) of the inkjet nozzles with respect to the polyimide substrate pattern. A line of PEDOT droplets is deposited into the hydrophilic regions at a distance d from the polyimide line that is sufficiently small for the spreading droplets to reach the repelling line. The lateral distance between successive droplets (10 to 20 μm) is smaller than the radius of sessile droplets (≈80 μm). Each droplet dries partially before the next droplet is deposited.

Atomic force microscopy (AFM) (Fig. 1B) shows that the inkjet-deposited PEDOT electrodes extend precisely up to the repelling polyimide line, whereas the second, unconfined boundary of the PEDOT line exhibits a typical roughness of ±10 μm (Fig. 1D). No PEDOT deposition occurs on top of the poly-

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imide. We have fabricated devices with channel lengths down to 5 μm, limited by the resolution of our photolithography setup. The AFM topographs suggest that fabrication of even shorter channels may be possible. The process is robust with respect to variations of the droplet volume or the distance *d*, which are caused by external perturbations of the droplet flight direction or changing ejection conditions at the nozzle. Device yields in our experiments, which were performed in a normal laboratory atmosphere, appear to be limited only by dust contamination. No evidence for accidental shorts between source and drain electrodes was found.

After IJP of source-drain electrodes, TFT devices are fabricated in a top-gate configuration (Fig. 1C) by spin-coating a continuous film (150 to 300 Å) of the active semiconducting polymer, poly(9,9-dioctylfluorene-co-bithiophene) (F8T2), from a xylene solution. Because of the low bulk conductivity of F8T2, no patterning of the semiconducting layer is required. A 400-to-500-nm–thick film of the gate dielectric polymer, polyvinylphenol (PVP), is spin-coated from isopropanol solution. Finally, a PEDOT/PSS gate electrode line overlapping the channel is inkjet printed in air.

The polyimide has a dual function. It not only provides accurate channel definition; when rubbed mechanically, it also acts as an aligning template for the self-organization of the semiconducting polymer that is crucial for achieving high field-effect mobilities. F8T2 is a rigid-rod polymer with a nematic liquid-crystalline phase above 265°C and can be aligned into a monodomain on top of the rubbed polyimide line by bringing it into the liquid-crystalline phase and subsequently quenching it (*10*). To make best use of fast intrachain transport along the polymer backbone, the chains are aligned uniaxially parallel to the direction of current flow (Fig. 1D). The field-effect mobility μ_{FET} extracted from the transfer characteristics (Fig. 2A) is μ_{FET} = 0.01 to 0.02 $cm^2/V{\cdot}s$, which is only 1 to 2 orders of magnitude lower than that of conventionally processed amorphous silicon TFTs. The mobility of printed F8T2 TFTs is similar to that of devices with photolithographically defined gold electrodes (*10*). This shows that through careful choice of the sequence of solvents and polymers to avoid dissolution and swelling of underlying layers, our printing process maintains the critical integrity and abruptness required of the different polymer-polymer interfaces in a multilayer TFT device.

Another important attribute of F8T2 [as opposed to regioregular poly-3-hexylthiophene with even higher mobilities of 0.1 $cm^2/V \cdot s$ (*6*)] is its relatively high stability against chemical doping by environmental oxygen or residual impurities such as mobile sulphonic acid in the PEDOT/PSS ink. This enables devices with higher on-off current ratios exceeding 10^5 and with better operating stability than printed poly-3-hexylthiophene devices (*11–13*). The threshold voltage $V_T \approx -10$ V, which is extracted from the *x*-axis intercept of the linear portion of the transfer characteristics ($V_{sd} = -4$ V), shifts by less than 1 V between subsequent gate voltage sweeps (Fig. 2A).

When comparing normalized drain currents $I_d \cdot L$ of devices with different channel lengths, approximate scaling of the device characteristics with *L* is observed (Fig. 2B). This confirms the successful printing of devices with channel lengths of 5 μm, as already suggested by AFM (Fig. 1). The normalized current of $L = 5$ μm devices is only slightly lower than that of $L = 20$ μm devices. The 5-μm devices exhibit less pronounced current saturation and a nonlinearity in the output characteristics at small source-drain voltages. This is attributed to contact resistance effects at the source-drain contacts that limit the current flow in devices with short channels and high currents. To quantify this parasitic contact resistance, we consider the fraction V_c of the applied source-drain voltage V_{sd} that drops across the source-

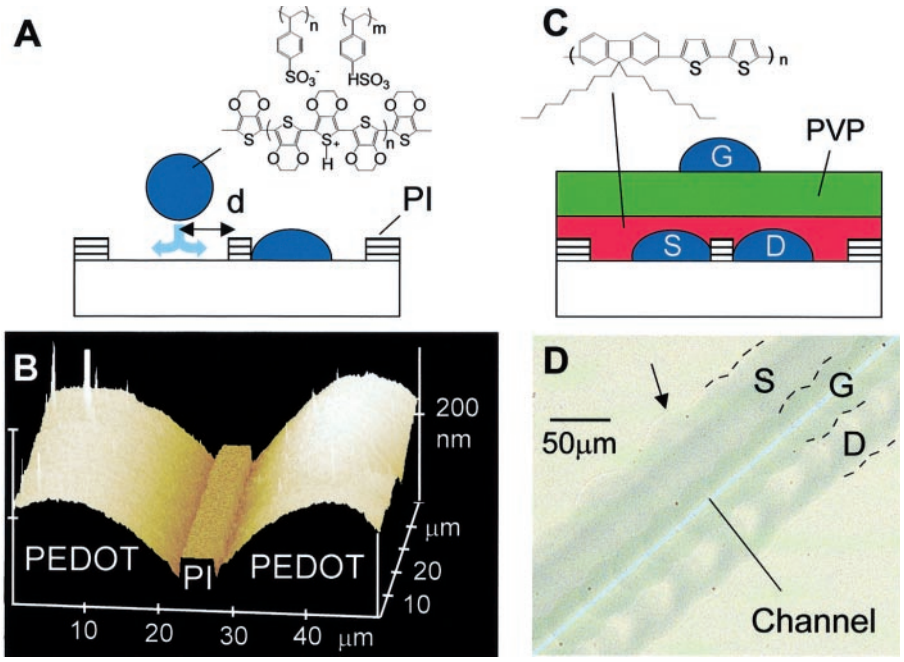

Fig. 1. (**A**) Schematic diagram of high-resolution IJP onto a prepatterned substrate. (**B**) AFM showing accurate alignment of inkjet-printed PEDOT/PSS source and drain electrodes separated by a repelling polyimide (PI) line with $L = 5$ μm. (**C**) Schematic diagram of the top-gate IJP TFT configuration with an F8T2 semiconducting layer (S, source; D, drain; and G, gate). (**D**) Optical micrograph of an IJP TFT ($L = 5$ μm). The image was taken under crossed polarizers so that the TFT channel appears bright blue because of the uniaxial monodomain alignment of the F8T2 polymer on top of rubbed polyimide. Unpolarized background illumination is used to make the contrast in the remaining areas visible, where the F8T2 film is in an isotropic multidomain configuration. The arrow indicates pronounced roughness of the unconfined PEDOT boundary.

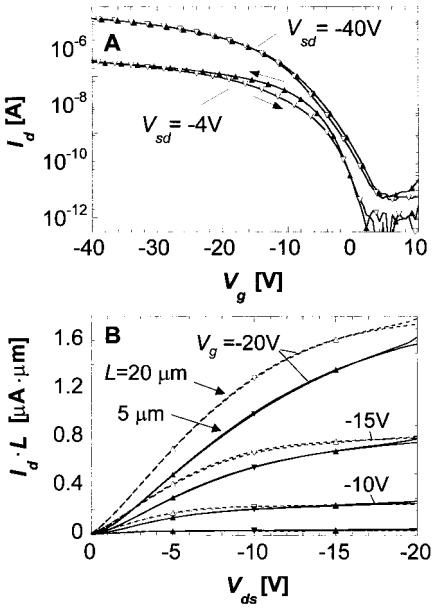

Fig. 2. (**A**) Transfer characteristics of an IJP TFT with F8T2 aligned uniaxially parallel to the current flow ($L = 5$ μm, $W = 3000$ μm) measured under an N_2 atmosphere. Subsequent measurements with increasing (solid symbols) and decreasing (open symbols) gate voltage are shown. (**B**) Scaling of the output characteristics of IJP F8T2 TFTs normalized by multiplying the drain current by the channel length (dashed lines with open symbols, $L = 20$ μm; solid lines with solid symbols, $L = 5$ μm). Subsequent measurements with increasing (upward triangles) and decreasing (downward triangles) gate voltage are shown.

drain contacts. The remaining voltage drop across the TFT channel is proportional to L. V_c depends only on the current I_d flowing through the contacts and on the gate voltage V_g, but not explicitly on L (*14*). We consider the linear operation regime ($V_{sd} \ll V_g$):

$$V_{sd}(L) = V_c(I_d, V_g) + \frac{I_d}{\mu_{FET} \cdot W \cdot C_i \cdot (V_g - V_T)} \cdot L \qquad (1)$$

C_i is the gate dielectric capacitance, and W is the channel width. By linear extrapolation of experimental $V_{sd}(L)$ values for fixed I_d and V_g of devices fabricated on the same substrate, we extract the current-voltage characteristics $I_c(V_c)$ (Fig. 3) (*15*). The contact resistance characteristics of devices with PEDOT electrodes are slightly nonlinear at voltages below 2 V, indicating a small energy barrier for hole injection at the PEDOT-F8T2 interface. However, at higher voltages the characteristics can be approximated by a constant parasitic resistance of, typically, 3 to 5 megohm. This resistance is mainly attributed to the limited bulk conductivity of the PEDOT source-drain lines, which is measured to be 1 to 2 S/cm (20 to 50 kilohm/square). Preliminary device modeling shows that a parasitic resistance of this order can consistently explain the deviations from ideal scaling behavior observed in Fig. 2B.

In comparison, devices fabricated with gold electrodes but with an otherwise identical configuration exhibit substantially more pronounced nonlinearities of the $I_c(V_c)$ (and output) characteristics with strongly reduced currents for $-V_{sd} < 0.5$ to 1 V (Fig. 3). At higher voltages, the characteristics rise more steeply, reflecting the higher conductivity of gold. The energy barrier for hole injection at the gold/F8T2 interface appears to be substantially higher than at the PEDOT/F8T2 interface, although PEDOT and gold have comparable workfunctions of about 5.1 eV (*16*). It is difficult to deduce quantitative information about injection barriers because of the complicated injection geometry and field configuration in the TFT, but similar observations have been reported for dark injection transient measurements on diode devices (*17*). We conclude that PEDOT/PSS provides more efficient hole injection into short-channel TFTs of rigid-rod conjugated polymers with high ionization potential (I_p = 5.5 eV for F8T2) than do inorganic metals of comparable workfunction. However, for high-mobility devices with $L < 5$ μm, higher bulk polymer conductivity is desirable.

To fabricate complex integrated transistor circuits by IJP, circuit components other than TFTs need to be developed as well. Of particular importance are via-hole interconnects, which provide electrical connections between electrodes and/or interconnects in different layers (*4*). We have developed an IJP process for integrated via-hole fabrication based on the local dissolution of materials by inkjet deposition of a good solvent. To fabricate a via-hole through a layer of PVP, for example, a droplet of isopropanol is deposited locally. The PVP dissolves and upon drying of the solvent redeposits on the side walls of a craterlike intrusion. This is repeated several times until the surface of the underlying layer, which also provides an automatic "etch stop," is exposed. Via-holes are filled by printing of PEDOT/PSS (Fig. 4A).

Via-holes are required for inverter devices: the basic building blocks of a logic circuit. Inverters can be implemented with two *p*-type transistors in either an enhancement-load or a depletion-load configuration (*18*). The enhancement-load configuration, in which the drain and gate of the load transistor are connected together through a via-hole (Fig. 4B), is appropriate for transistors that are normally off such as inkjet-printed F8T2 devices ($V_T \approx -10$ V, Fig. 2A). Alternatively, inverters with a printed resistor as the load element have been used. Resistors are fabricated by IJP of a line of PEDOT/PSS with a resistance value that can be adjusted over a wide range by varying the concentration of PSS. In both configurations, clean inverter action is observed for switching between logic "1" (−20 V) and logic "0" (0 V). The hysteresis of the characteristics is small, reflecting the stability of the transistor threshold voltage. The voltage gain $\frac{dV_{out}}{dV_{in}} \approx 2$ is

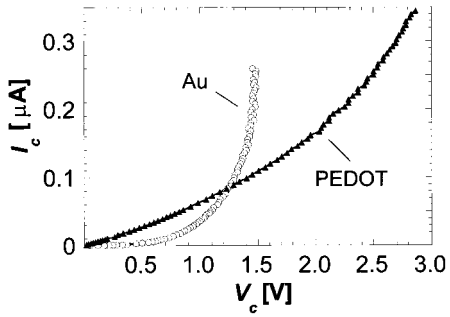

Fig. 3. Current-voltage characteristics of the parasitic source-drain contact resistance for IJP PEDOT (solid triangles) and gold electrodes (open circles). The gold source-drain electrodes were cleaned carefully by exposure to O_2 plasma before deposition of F8T2.

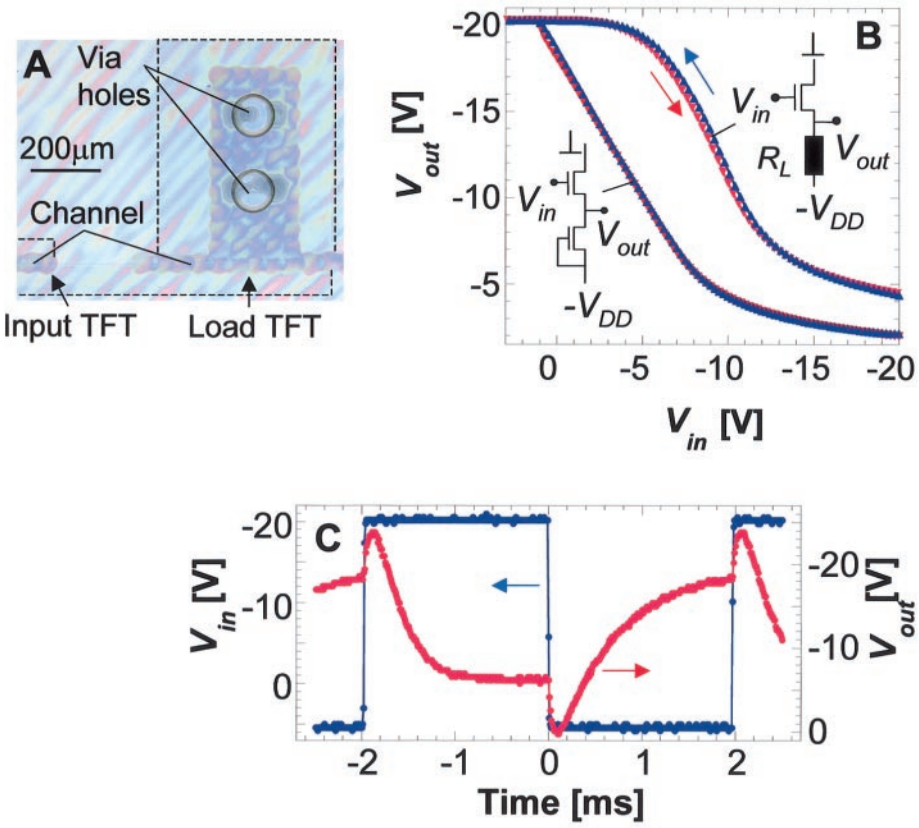

Fig. 4. (**A**) Optical micrograph of two via-holes connecting the drain and gate electrodes of the load TFT in an enhancement-load IJP inverter (L = 5 μm). Some reddish interference contrast is seen due to small spin-coating–induced thickness variations of the PVP dielectric. (**B**) Static characteristics of an enhancement-load inverter (L = 5 μm, width of the input switching transistor W_I = 2150 μm, and width of the load transistor W_L = 450 μm) and of a resistance-load inverter (L = 5 μm, W_I = 2150 μm, and R_L = 47 megohm) measured with increasing (red) and decreasing (blue) input voltage V_{in} (negative supply voltage V_{DD} = 20 V). (**C**) Dynamic switching characteristics of the resistance-load inverter in (**B**) (ν_{in} = 250 Hz). The spikes of the output voltage after abrupt switching of the input voltage are induced by direct capacitive coupling on the TFT substrate between input and output electrodes.

larger than 1, implying that these gates can be used to switch subsequent stages in more complex logic circuits. Higher gains of 5 to 7 have been obtained by increasing the load resistance.

Inkjet-printed inverters can be switched at frequencies up to a few hundred hertz, as shown in Fig. 4C for the resistor-load device of Fig. 4B. The fall time $\tau_{1\rightarrow0} = 350$ μs is determined by the on current of the input transistor and by the load capacitance of our measurement setup ($C_L \approx 20$ pF). The rise time $\tau_{1\rightarrow0} = 750$ μs was designed to be comparable to the fall time by adjusting the load resistance ($R_L = 47$ megohm). We estimate the total power consumption of an inverter stage, as in Fig. 4B, to be about 2 μW when switching five subsequent inverter stages (fanout = 5) at a frequency of 250 Hz (*18*). Further improvements are expected from increasing polymer mobility and PEDOT conductivity, and reducing channel length and source-drain-to-gate overlap capacitance ($C_{sd\text{-}g} \approx 5$ pF for $W = 2000$ μm).

The performance of our inkjet-printed, all-polymer TFT circuits is believed to be adequate for applications such as active-matrix displays or identification tags. The TFT performance and the inverter switching speed are comparable to that of all-polymer TFT circuits reported by the Philips group who used a three-level photolithographic process to pattern electrodes and via-holes (*4, 19*). We believe that our IJP process will allow a similar degree of circuit complexity. IJP has advantageous attributes that will be required for continuous reel-to-reel processing of large-area circuits on plastic substrates. Because only a hydrophobic/hydrophilic surface energy contrast but no topographic profile is required for ink confinement, the photolithographic substrate prepatterning using polyimide can easily be replaced by soft lithography or photopatterning of a self-assembled monolayer (*20*), so that the entire circuit fabrication, including via-hole interconnections consists only of successive solution coating and printing steps. Particular advantages of IJP are as follows: (i) Different materials can be delivered simultaneously from multiple nozzles. (ii) IJP provides accurate registration over large areas, because the inkjet head can be aligned locally with respect to a previously deposited pattern. The local registration, which can be automated, is particularly important for flexible substrates, which inevitably exhibit distortions. (iii) Application- or even end-user–specific circuits can be defined by simple IJP of a network of interconnections and via-holes on a prefabricated array of transistor gates.

The physical mechanism underlying the precise self-alignment of inkjet-printed electrodes with the hydrophobic confinement structure is complex. It involves the simultaneous dynamic processes of droplet spreading and solidification, resulting in an increase of viscosity in the advancing front of the droplet (*21*). Our dynamic, nonequilibrium droplet deposition technique overcomes inherent problems associated with forming high-resolution features by liquid-phase deposition onto patterned substrates. In static equilibrium, liquid patterns suffer from problems such as bulge formation (*22*), capillary breakup, or a sensitive dependence of film thickness on the shape and size of the pattern (*23*). None of these problems occurred in the IJP process, which allows precise local control of deposited droplet volume and drying time to form patterns with arbitrary shape and thickness. The submicrometer precise alignment observed in AFM topographs (Fig. 1A) suggests that our process can be extended to definition of even finer, possibly submicrometer features.

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13 September 2000; accepted 6 November 2000

Ultrahigh-Density Nanowire Arrays Grown in Self-Assembled Diblock Copolymer Templates

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We show a simple, robust, chemical route to the fabrication of ultrahigh-density arrays of nanopores with high aspect ratios using the equilibrium self-assembled morphology of asymmetric diblock copolymers. The dimensions and lateral density of the array are determined by segmental interactions and the copolymer molecular weight. Through direct current electrodeposition, we fabricated vertical arrays of nanowires with densities in excess of 1.9×10^{11} wires per square centimeter. We found markedly enhanced coercivities with ferromagnetic cobalt nanowires that point toward a route to ultrahigh-density storage media. The copolymer approach described is practical, parallel, compatible with current lithographic processes, and amenable to multilayered device fabrication.

Continued advances in technologies such as magnetic storage and optoelectronics depend crucially on the ability to produce ultrahigh-density arrays of nanometer-scale elements (*1–11*). As critical device dimensions shrink to the nanometer scale, the parallel fabrication of well-ordered arrays becomes increasingly difficult. We demonstrate a method to rapidly and reliably fabricate arrays with densities in excess of 1 terabit per square inch, based on the self-assembled morphology in diblock copolymer thin films. An ordered, nanoporous structure obtained from the copolymer film by chemical modification is

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