A Polymer Transistor Circuit Using PDHTT

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***Abstract*—A digital circuit using polymer thin-film transistors on polyester substrate is presented. The circuit consists of 171 transistors and converts a parallel word of four bits into a serial bit sequence by use of gates and flip-flops with level shifters. The integrated clock generator runs at oscillation frequencies of approximately 200 Hz with supply voltages of −25 V/+12 V. The polymer poly(3,3″-dihexyl-2,2′:5′,2″-terthiophene) (PDHTT) is used as semiconducting material. Measurement results for the circuit demonstrate that PDHTT can be used for digital polymer circuits.**

***Index Terms*—Counting circuits, digital integrated circuits, flip-flops, organic semiconductor, plastic electronics.**

I. Introduction

TRANSISTORS with polymer semiconducting materials have been a research subject for almost three decades now. These devices are of interest for low-cost applications such as smart price tags. A first complex circuit using organic transistors was demonstrated by Philips [1] that implemented a 15-bit code sequence generator using p-type semiconducting pentacene. The oligomer pentacene is commonly evaporated in vacuum. More interesting in terms of cheap processing technologies are long-chain polymers that can be homogeneously cast [2] from solution by spincoating, or can even be printed on substrates by traditional or jet printing [3]. Polymer poly-(3-alkylthiophene) transistors with switching gate delays as low as 0.68 μs at supply voltages of 80 V [4], and operation lifetimes of more than 1000 h [5] have been reported.

In this letter, the polymer poly(3,3″-dihexyl-2,2′:5′,2″-terthiophene) (PDHTT) [6] is evaluated for its suitability for digital polymer circuits. A digital integrated circuit using p-type semiconducting PDHTT is presented. The circuit works as a four-bit parallel-to-serial converter and continuously issues the four bits of a dynamically programmable code in sequential order. To our knowledge, it is the first circuit reported to use PDHTT as semiconducting material.

II. Device Fabrication

The four-bit parallel-to-serial converter is based on top-gate thin-film transistors using soluble polymers for the semiconducting and the insulating layers. The substrate is a flexible polyester film, and the drain/source layer, which consists of a 40–nm gold layer, was sputtered directly on it. Using commercially available photoresist and developer, the drain/source electrodes are patterned by standard photolithography. On top of this, the soluble semiconducting polymer PDHTT is applied by a spincoating technique to produce a layer that is approximately 35 nm thick. For this the semiconductor was solved in chloroform. As an insulating layer an organic copolymer blend with a relative dielectric constant of 3.5 was dissolved in dioxane and spincoated on top of the semiconducting layer. This procedure results in an homogeneous 300-nm-thick layer without pin holes. To enable vertical interconnects (vias), holes in the semiconducting and the insulating layers are realized by photolithography. The devices are completed by a 40-nm gold layer for the gate electrodes using sputtering and photolithography. The whole process was performed under clean room conditions in the presence of oxygen and humidity. The devices were not encapsulated and were stored and measured under ambient conditions. The semiconducting material was synthesized and supplied by the group of Prof. Gallazzi at the Polytechnic University of Milan, Milan, Italy. Details can be found in [7]–[9].

III. Circuit Description

A demonstration circuit has been realized using 171 depletion-mode p-channel PDHTT transistors. The circuit is composed of a clock generator, a two-bit counter, four latches as static memory cells, and a four-bit multiplexer.

The most basic gate in the circuit is the inverter. Fig. 1 shows the schematic and measured voltage transfer characteristics of the implemented gate as well as drain current versus drain-source voltage characteristics of a transistor. In order to improve gate behavior, the inverting stage (transistors M1/M2) is followed by a level shifter configuration (M3/M4) [10], [11]. Device widths for transistors M1 to M4 are $W1 = 1$ mm, $W2 = 5$ mm, $W3 = 3$ mm, and $W4 = 2$ mm. Each transistor has a channel length of 5 μm.

The level shifter M3/M4 pushes the output of the inverting stage to more positive voltages. Without this block, only output voltages below 0 V would be possible, and the logic level close to 0 V could not reach its saturation region. Fig. 2 shows the schematic of the converter circuit and Fig. 3 shows a layout photograph. A ring oscillator consisting of seven inverters in a row generates the complementary clocking signals CLK and $\overline{\text{CLK}}$. These clocking signals are fed into a two-bit counter that

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consists of four clocked set/reset flip-flops (SR-FFs). These SR-FFs form two master-slave flip-flops (MS-FFs). The master

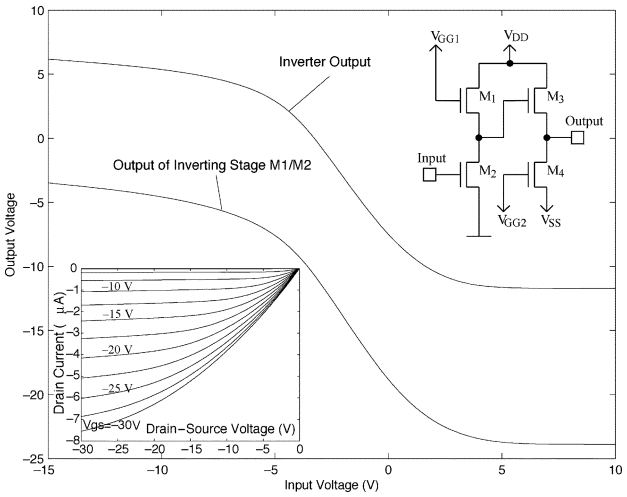

Fig. 1. Transfer characteristics and schematic of the inverter. Supply voltages for the transfer characteristics are $V_{\rm DD} = V_{\rm GG1} = -25$ V, and $V_{\rm GG2} = 0$ V, $V_{\rm SS} = +12$ V. The lower inset shows drain current versus drain-source voltage characteristics at various gate-source voltages for a PDHTT transistor with a channel width of 10 mm and a channel length of 10 μm at $V_{\rm GS} = 0$ V, -2.5 V, $\ldots$, -30 V. The device has a mobility of $3 \cdot 10^{-3}$ cm^2/V·s, a subthreshold slope of 1.35 V/dec, a drain current on/off ratio of 10^4 (measured at a drain-source voltage of -0.1 V and gate-source voltages between $+1$ V and -20 V), and a threshold voltage of -1 V.

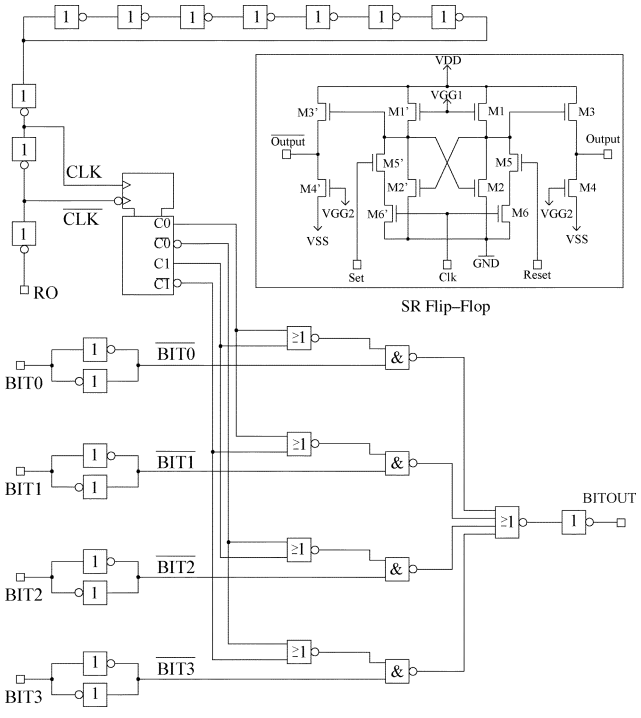

Fig. 2. Schematic of the four-bit parallel-to-serial converter circuit. The inset shows the schematic of an SR flip-flop cell, which is the basic building block for the two-bit counter.

and slave stage of each MS-FF are driven by CLK and $\overline{\rm CLK}$, respectively. The inset in Fig. 2 shows a schematic view of the

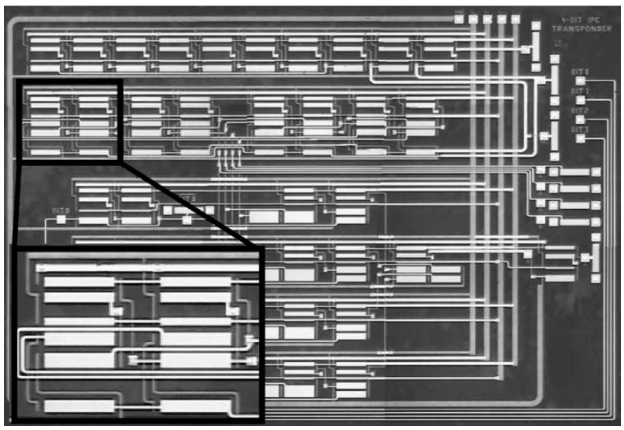

Fig. 3. Photograph of the four-bit parallel-to-serial converter circuit. The circuit size is 10.7 × 7.3 mm. The inset in the lower left corner shows a magnified view of one of the SR flip-flops.

SR-FF. The transistor dimensions are based on the basic inverter gate with the additional devices M5/M5′ and M6/M6′ having widths of 4 mm each. The four memory cells in the circuit are each built from two inverters forming a latch. Each cell can be programmed by applying a voltage representing the desired logic state at the corresponding input pad. NAND gates, NOR gates, and a final inverter gate constitute the four-bit multiplexer.

IV. Experimental Results

The transient behavior of the circuit has been measured. Supply voltages for the circuit are $+12$ V for the positive supply $V_{\rm SS}$ and -25 V for the negative supply $V_{\rm DD}$. $V_{\rm GG1}$ is connected to $V_{\rm DD}$, and $V_{\rm GG2}$ is connected to 0 V. This voltage configuration gives rise to stable logic levels and an oscillation frequency of about 200 Hz. Oscillation starts with approximately 100 Hz at voltages of $+4$ V for the positive supply and -10 V for the negative supply. Fig. 4 shows the clocking signal and data outputs of the circuit when a bit sequence of (High, High, High, High), (Low, High, High, High), and (Low, High, Low, High), respectively, has been programmed. In this letter, the output voltage level closer to the negative supply voltage $V_{\rm DD}$ is regarded as the logic high state, and the voltage level closer to the positive supply voltage $V_{\rm SS}$ is regarded as the logic low state.

V. Conclusion

A four-bit parallel-to-serial converter based on depletion-mode p-channel devices has been demonstrated in this work. The circuit consists of 171 polymeric PDHTT transistors and uses logic gates and flip-flops with level shifters. The experimental results in this letter show that digital circuits can be built with polymeric PDHTT as semiconducting material.

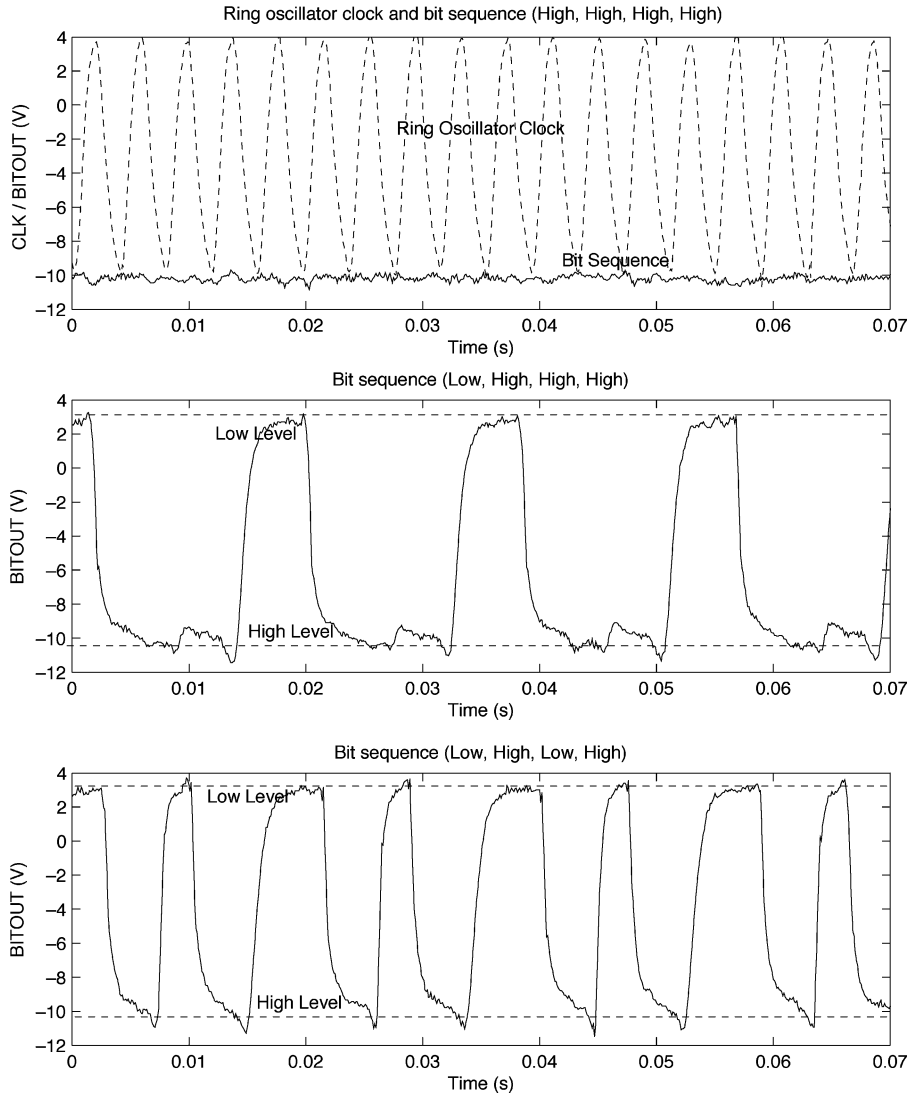

Fig. 4. Output measurement for code sequences (High, High, High, High), (Low, High, High, High), and (Low, High, Low, High). Supply voltages are $V_{\rm DD} = {\rm VGG1} = -25$ V, $V_{\rm GG2} = 0$ V, and $V_{\rm SS} = +12$ V. The topmost graph also shows the clocking signal generated by the ring oscillator in the circuit.

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